ARGUMENTS/REMARKS

Reconsideration of the above-identified application in view of the following is respectfully requested. Claims 26-32 are pending.

Claims 27 and 28 stand rejected under 35 U.S.C. 101 as lacking utility because the first communication section is not connected to another device and a second communication sections is not connected to another device. Claims 27 and 28 also stand rejected under 35 U.S.C. 112 since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above. These rejections are respectfully traversed.

Claim 26 is directed to a device having first and second communication sections which are suitable for connection to similar devices. Claim 26 does not recite that the first and second communication sections can communicate to other devices. Claims 27 and 28 depend on claim 26 and recite clock logic levels held as outputs by the first and second communication sections of claim 26 when they are not connected to other devices. As is explained in the description of the applicant's specification at page 24, line 20 to page 25, line 25 with reference to Fig. 10, the clock logic levels held as outputs by the first and second communication sections provide the advantage that when the two devices, according to the claims, are connected together through their respective first and second communication sections, an oscillating loop providing a clock signal to control communications between the two devices is immediately and automatically established. Further, as explained at page 25, lines 19-25, it is also advantageous that the first and second communication sections are held at a

constant voltage when not connected so that the unconnected communication sections do not generate electromagnet interference. Also, claims 27 and 28 define devices that can be connected to other similar devices for communication therebetween.

Therefore, in view of the above reasons, the claimed inventions of claims 27 and 28 have utility and thus, the rejections of claims 27 and 28 under 35 U.S.C. 101 and 35 U.S.C. 112 should be withdrawn.

Claims 26-32 stand rejected under 35 U.S.C. 102(e) as being anticipated by Haq. This rejection is respectfully traversed for the following reasons.

Haq does not disclose or suggest the subject matter of a first communications section arranged to respond to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along the first communications link, and a second communications section arranged to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link. Haq shows in figure 19 a plurality of devices 1905 and 1920 connected together by buses. As is clearly shown in figure 19, the bus includes a conductor 1920, which carries a clock signal from a clock source 1915 to all of the devices 1905, 1910 located along the bus. The direction of propagation of the clock signal is indicated by an arrow in figure 19.

The examiner suggests that the text at column 18, line 54 to column 20, line 40 of Haq discloses the above-mentioned subject matter of claim 26.

However, this subject matter is not disclosed by Haq. Haq explicitly states at column 18, lines 56-60 that "the system clock bus 1920 starts from a clock source 1915 at the end opposite the memory controller 1905, is connected to all devices 1910 and terminates at the memory controller 1905". In Haq, the clock signal is simply sent along the system clock conductor 1920 from a clock source at one end to a termination (VDT) at the other end and all of the devices 1905 and 1910 simply detect the clock signal and use it to synchronize the sending of data and other signals along the other bus conductors.

There is no disclosure in Haq of the individual devices 1905, 1910 sending clock signals to one another. In the embodiment of figure 19 and all of the other embodiments, all clock signals are generated by a clock source separate from the devices 1905, 1910, and the clock source sends the clock signals along continuous conductors of the bus from one end of the bus to the other. Haq does not disclose or suggest that the devices 1905, 1910 connected to the bus, and in particular connected to the clock conductor 1920 should respond to reception of clock transition signals along first and second communication links by transmitting transition signals back along the communication links as defined in claim 26.

The Examiner has specifically cited the phrase "opposite polarity". However, this phrase is found in the examiner's referenced section of Haq only at column 19, line 13 to refer to a reference signal /SSVTR1 having the opposite polarity to a reference signal SSVTR1. These reference signals SSVTR1 and /SSVTR1 are entirely separate from the clock signal as can clearly be seen in

figure 19 where the reference signals SSVTR1 and /SSVTR1 are shown carried by different conductors of the bus to the clock signal.

The signals SSVTR1 and /SSVTR1 are not clock signals. These signals are reference signals used by comparators in the devices 1910 as references compared to data signals. The SSVTR and /SSVTR signals are generated within the master device 1905 and the SSVTR and /SSVTR signals are not clock signals. It is explained at column 19, lines 34 to 40 that these signals may be derived from the clock signal.

It is explained at column 14, lines 7 to 14 of Haq that The master 1305 transmits on SSVTR and /SSVTR lines 1340 a first set of SSVTR and /SSVTR references and a second set of SSVTR and /SSVTR references to the slaves 1310. That is, the SSVTR and /SSVTR reference signals are generated by the controller and transmitted along conductors of the bus to all of the slave devices.

Moreover, even if the reference signals SSVTR and /SSVTR were regarded as clock signals, because they are transmitted from the controller along conductors of the bus and sensed and used as reference signals by the slave devices, there is no disclosure in Haq of communication sections being arranged to respond to a clock transition signal along the first communication link by transmitting a clock transition signal having the same polarity back along the first communications link and a second communication section arranged to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link as required by claim 26. In Haq, the signals are

simply sent and used as references by the slave devices. Haq does not disclose or suggests that the slave devices could respond to these signals by transmitting a signal back along the communication link according to claim 26. Thus, claim 26 is not anticipated or made obvious by Haq. Therefore, in view of the above-mentioned reasons, claim 26 is allowable.

Claim 27, which depends on claim 26, should be allowed for the same reasons as claim 26 and also for the additional feature that the first communications section holds a first clock logic level and an output, when the first communications section is not connected to another device, and the second communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an input, when the second communications section is not connected to another device. Haq does not disclose or suggest this feature.

Claim 28, which depends from claim 26, should be allowed for the same reasons as claim 26 and also for the additional feature that the second communications section holds a first clock logic level as an output, when the second communications section is not connected to another device, and the first communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an output, when the first communications section is not connected to another device. Haq does not disclose or suggest this feature.

In items 6 and 7 of the office action, it is suggested that claims 27 and 28 are disclose in Haq. Applicant respectfully disagrees. Claims 27 and 28 relate to

alternative arrangements of the device of claim 26 and define respective relationships between the clock logic levels held as an output by the first and second communications sections of the device when the communication sections are not connected to another device. It is submitted that there is no disclosure in Haq relevant in any way to the relationship between the clock logic levels having outputs in claims 27 and 28.

Specifically, in Haq, the clock signal and the reference signals are all transmitted by their sources along different conductors of the bus. The clock signal is transmitted from the clock source and the SSVTR and /SSVTR signals are transmitted from the controller. These clock and reference signals are detected by the devices 1910. As explained above, the devices 1910 do not respond to reception of any of these signals by the transmitting the signal back in the opposite direction. Accordingly, because the devices 1910 are arranged only to receive signals and not to resend them, the devices 1910 do not have any parts holding a clock logic level as an output. Therefore, claims 27 and 28 are allowable.

Claim 29, which depends from claim 26, should be allowed for the same reasons as claim 26 and also for the additional feature that the linked communication sections form a loop, when the first communications section is linked to the second communications section of another device or vice-versa through a bi-directional communications link, and wherein the device uses an oscillating clock transition signal passing around the loop as a clock signal for communication along the communications link. Haq does not disclose or suggest

this feature. No such loop having an oscillating loop transition signal passing around it is disclose anywhere in Haq. Haq merely shows a number of clock signal arrangements. In figure 19, a clock signal from a clock source 1915 passes along a signal conductor 1920 on the bus and terminates at a resistor VTT. A related system is shown in figure 20 where two clock signals travel in parallel in the same direction along two different conductors 1920 of a multiple bus. The two clock signals are both generated by a clock source 1915 and terminate at respective resistors VTT.

Further, figures 21 and 24 show arrangements in which a clock signal from a clock source 21 and 32 passes in a first direction along a first conductor 21 and 36. The clock signal transfers to a second conductor 21 to 38 and passes along the bus in the opposite direction. The clock signal then terminates at a resistor.

In all of these arrangements, the clock signal starts from a clock source and travels linearly to a terminal resistor. There is no disclosure in Haq of a clock signal traveling around a loop.

The Examiner refers to the use of a phase-locked loop in Haq. This phase-locked loop is referred to at column 14, lines 23 to 25, which explains that the phase-locked loop is used to lock the clock frequency and timing. Use of a phase-locked loop to produce a timing signal as suggested in Haq does not disclose or suggest to the person skilled in the art the possibility of linked communication sections connected through a bi-directional communication link and using an oscillating clock transition signal passing around the loop as a clock signal for

communication along the communication link according to claim 29. Therefore, claim 29 is allowable.

Claim 30, which depends from claim 29, should be allowed for the same reasons as claim 29 and also for the additional feature that when the first and second communication sections are first linked, the difference between their held input and output clock logic levels causes the oscillating clock transition signals to begin passing around the loop. Haq does not disclose or suggest this feature. Figures 6 and 7 of Haq show various signal processing circuits but none of these circuits includes any loop which an oscillating clock signal could pass around. Further, figures 6 and 7 show different circuit configurations and the description text explains how theses circuits react to different applied signals. There is no disclosure in Haq regarding the behavior of the circuit elements shown in figures 6 and 7, when disconnected from other circuit elements or any explanation as to how they would react when they were first connected. Therefore, claim 30 is allowable.

Claim 31 is directed to an electronic communication network comprising at least first and second devices connected by at least one bi-directional communications link, wherein a loop is formed by the first device receiving a clock transition signal along the communications link and sending a clock transition signal having the same polarity back along the communications link and the second device receiving a clock transition signal along the communications link and sending a clock transition signal having the opposite polarity back along the communications link. The first and second devices use the oscillating clock

transition signals traveling around the loop to provide a clock signal to control data transfer along the communications link. Haq does not disclose or suggest all of the features recited in claim 31.

Haq shows in figure 19 a plurality of devices 1905 and 1920 connected together by buses. As is clearly shown in figure 19, the bus includes a conductor 1920, which carries a clock signal from a clock source 1915 to all of the devices 1905, 1910 located along the bus. The direction of propagation of the clock signal is indicated by an arrow in figure 19. The examiner suggests that the text at column 18, line 54 to column 20, line 40 of Haq discloses the above-mentioned subject matter of claim 31. However, this subject matter is not disclosed by Haq. Haq explicitly states at column 18, lines 56-60 that "the system clock bus 1920 starts from a clock source 1915 at the end opposite the memory controller 1905, is connected to all devices 1910 and terminates at the memory controller 1905". In Haq, the clock signal is simply sent along the system clock conductor 1920 from a clock source at one end to a termination (VDT) at the other end and all of the devices 1905 and 1910 simply detect the clock signal and use it to synchronize the sending of data and other signals along the other bus conductors.

There is no disclosure in Haq of the individual devices 1905, 1910 sending clock signals to one another. In the embodiment of figure 19 and all of the other embodiments, all clock signals are generated by a clock source separate from the devices 1905, 1910, and the clock source sends the clock signals along continuous conductors of the bus from one end of the bus to the other. Haq does not disclose or suggest that the devices 1905, 1910 connected to the bus, and in

particular connected to the clock conductor 1920 receive clock transition signals along the communications link and send clock transition signals back along the communications link as defined in claim 31.

The Examiner has specifically cited the phrase "opposite polarity". However, this phrase is found in the examiner's referenced section of Haq only at column 19, line 13 to refer to a reference signal /SSVTR1 having the opposite polarity to a reference signal SSVTR1. These reference signals SSVTR1 and /SSVTR1 are entirely separate from the clock signal as can clearly be seen in figure 19 where the reference signals SSVTR1 and /SSVTR1 are shown carried by different conductors of the bus to the clock signal.

The signals SSVTR1 and /SSVTR1 are not clock signals. These signals are reference signals used by comparators in the devices 1910 as references compared to data signals. The SSVTR and /SSVTR signals are generated within the master device 1905 and the SSVTR and /SSVTR signals are not clock signals. It is explained at column 19, lines 34 to 40 that these signals may be derived from the clock signal.

It is explained at column 14, lines 7 to 14 of Haq that The master 1305 transmits on SSVTR and /SSVTR lines 1340 a first set of SSVTR and /SSVTR references and a second set of SSVTR and /SSVTR references to the slaves 1310. That is, the SSVTR and /SSVTR reference signals are generated by the controller and transmitted along conductors of the bus to all of the slave devices.

Moreover, even if the reference signals SSVTR and /SSVTR were regarded as clock signals, because they are transmitted from the controller along

conductors of the bus and sensed and used as reference signals by the slave devices, there is no disclosure in Haq of a loop formed by a first device receiving a clock transition signal along the communications link and sending a clock transition signal having the same polarity back along the communications link and a second device receiving a clock transition signal along the communications link and sending a clock transition signal having the opposite polarity back along the communications link as required by claim 31. Haq does not disclose any such clock transition signal traveling around a loop at all.

In Haq, the signals are simply sent and used as references by the slave devices. Haq does not disclose or suggest that the slave devices could receive a clock transition signal and send a clock transition signal back along the communication link according to claim 31. Thus, claim 31 is not anticipated or made obvious by Haq. Therefore, in view of the above-mentioned reasons, claim 31 is allowable.

Claim 32, which depends from claim 31, should be allowed for the same reasons as claim 31 and also for the additional feature that the clock transition signals traveling around the loop are used as the clock signal. Haq does not disclose or suggest this feature. Therefore, claim 32 is allowable.

In view of the foregoing, it is respectfully requested that the amendment be entered and the application allowed. Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

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